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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants

Andy L. Lee, Brian Johnson,

and Richard G. Cliff

Application No.:

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For

SHIFT REGISTER IMPLEMENTATIONS OF

FIRST-IN/FIRST-OUT MEMORIES

RECEIVED

Group Art Unit:

2818

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Technology Center 2100

Hon. Commissioner for Patents Washington, D.C. 20231

INFORMATION DISCLOSURE STATEMENT

Sir:

In accordance with 37 C.F.R. §§ 1.56 and 1.97, applicants wish to call the attention of the Examiner to the following references:

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- P. Chow et al., "A 1.2µm CMOS FPGA using Cascaded Logic Blocks and Segmented Routing", <u>FPGAs</u>, Chapter 3.2, pp. 91-102, W.R. Moore and W. Luk (eds.), Abingdon EE&CS Books, Abingdon, (UK), 1991.
- L. Mintzer, "FIR Filters with the Xilinx FPGA", FPGA '92 #129-#134.
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- "XC4000E and XC4000X Series Field Programmable Gate Arrays; Product Specification", May 14, 1999 (Version 1.6), Xilinx Inc., San Jose, CA, pp. 6-5 through 6-72.

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"Triscend E5 Configurable System-on-Chip Family", Triscend Corporation, January 2000 (Version 1.00) Product Description, cover page and pp. 25-28.

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"Virtex 2.5V Field Programmable Gate Arrays", DS003 (v. 2.0), Preliminary Product Specification, March 9, 2000, Xilinx, Inc., San Jose, CA, pp. 1-72.

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These references are also listed on the attached Form PTO-1449, and copies are enclosed.

Consideration of the foregoing in relation to this patent application is respectfully requested.

Respectfully submitted,

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